REMARKS/ARGUMENTS

Favorable consideration of this application in light of the following discussion is respectfully requested.

Claims 1-4 are pending in this application.

In the outstanding Office Action, Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee (U.S. Patent 5,426,447) in view of Masahiko (Japanese Patent Publication No. 63-261326); Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Masahiko in view of Kwon (U.S. Patent No. 5,850,216); Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Masahiko in view of Koyama et al. (U.S. Patent No. 6,177,920; hereinafter Koyama); and Claim 3 was indicated as containing allowable subject matter.

Briefly recapitulating, the present invention is directed to a process for displaying data on a matrix display having N data lines and P selection lines. At the intersections of the data lines and selection lines are image points or pixels. The N data lines are grouped into P blocks of N' data lines (N = P x N'). Each block receives in parallel one of the P data signals, for instance DB1. The data signal applied on a block is demultiplexed on the N' lines of the block, by successively scanning each one of the N' lines. This scanning operation of the data lines in each block is alternately done from 1 to N' and from N' to 1 according to which selection line is currently selected. This allows for a display without introducing a DC error of several tens of mV along a selection line between the first column sampled in the block and the last, as is common in conventional systems.[1]

Applicants' Figure 1 shows an exemplary configuration of N data lines (columns) divided into P blocks of N' data lines (e.g., N'= 9 and data lines C1-C9 belong to one of the P blocks), and M selection lines (e.g., row lines L1 – L4). Each block receives in parallel one

[1] Specification, page 3, lines 11-21.

of the P data signals. The data signal applied on a block is demultiplexed by sampling signals (DW1 – DW9) on the N' data lines (e.g on C1 to C9). The timing of the sampling signals is controlled so that ~~for~~ the claimed patterns of forward and backward scans are performed.[2]

Lee discloses a method for demultiplexing Y data selection signals over X groups of Y data lines. In particular, Lee discloses pixels located at the intersection of data lines and row lines.[3] In Lee, the number of data lines is equal to the number of groups multiplied by the number of data lines/group.[4] As noted in the Office Action,[5] Lee does not disclose alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines, as recited in Applicants' Claim 1.

Masahiko discloses a driving circuit for an electro-optic device where brightness differences are averaged by alternately leading out electrode lines of column group 3 on left and right [columns] (e.g. the select pulse 13 is applied by their left side over odd gate lines, and by their right side over even gate lines) and reversing the vertical scanning order of select pulses supplied to the left column electrode line group 3 (e.g., every line is scanned downward) from the scanning order of select pulses supplied to the right column electrode line group 3 (e.g., every line is scanned upward).[6]

However, contrary to the Official Action, Masahiko, like Lee, does not disclose alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines as recited in Applicants' Claim 1. In Masahiko, the select pulse 13 is applied to right column electrode lines group 3 by their right side, and the lines of this right group are scanned in a first vertical direction (e.g., upward) while the select pulse 13 is applied to left column electrode line group 3 by their left side, but the lines of this left group

[2] Specification, page 4, line 27 – page 5, line 16.
[3] Lee, column 5, lines 31-37 and column 6, lines 33-41.
[4] Lee, column 6, lines 48-60.
[5] Office Action, page 6, lines 3-4.
[6] Masahiko, page 8, lines 20-26.

are scanned in an opposite vertical direction (e.g., downward). That is, in Masahiko, the vertical scanning direction of the electrode lines of group 3 is reversed for alternate lines. Furthermore, in Masahiko, there is no link between the electrode line (gate line) of group 3 which is currently selected and the driving mode of the electrode lines of group 4 applied by driver 2. Thus, Masahiko cannot alternately scan from 1 to N' and from N' to 1 according to which selection line is currently selected as recited in Applicants' Claim 1.

To further explain, Masahiko addresses a problem of "gradational display" between the bottom and the top of the image.[7] Gradational display is related to leakages in TFT's (i.e., the problem of the "OFF condition" of selection transistors[8] or to parasitic capacitance such as pixel-column capacitance. Thus, Masahiko seeks to obtain "*a good display quality without striking brightness irregularity.*"[9] This problem is found in an active matrix with a frame inversion addressing mode. To solve this problem Masahiko discloses addressing odd gate lines (i.e., selection lines) from the left side and even gate lines (i.e., selection lines) from the right side.[10] Masahiko also discloses under title "*Actual Example*": "*alternately leading out column electrodes lines on left and right.*"[11] Masahiko further proposes, for a particular frame, **to invert the scanning sense**, so that the electrode lines (gate lines) accessed from the left side are scanned **downwardly** from top down to bottom (see arrow ↓ on Figure 1 of Masahiko) and the electrode lines (gate lines) accessed from the right side are scanned **upwardly** from bottom to top (see arrow ↑ on Figure 1 of Masahiko). Masahiko also discloses under title *Actual example*: "*reversely setting the scanning order* of select pulses supplied to left column electrode line group and the scanning order of select pulses supplied

[7] Masahiko, page 5, lines 1-20.
[8] Masahiko, page 6, last paragraph.
[9] Masahiko, page 3, first paragraph.
[10] Masahiko, Figure 1.
[11] Masahiko, page 8.

to right column electrode line group."[12] By these means "brightness differences are averaged *by rearranging the scanning order of address signals.*"[13]

However, the rearranging (i.e., "reversely setting") of the scanning order of address signals disclosed by Masahiko is clearly different from the claimed invention, wherein the scanning order of the data lines in a block is changed according to which selection line is currently addressed. That is, Masahiko exclusively discloses alternate vertical scanning of gate lines and does not disclose or suggest alternate scanning of data lines in a block, according to which selection line (gate line) is currently addressed, as recited in Applicants' Claim 1. However, in Applicants' claimed invention, in each of the P blocs, the data lines (or columns) are scanned from left to right side (from 1 to N') or inversely (from N' to 1), as a function of which selection line is currently addressed. While alternating the horizontal scanning pattern of the N' data lines of a block from 1 to N' and from N' to 1, the selection lines are common for the whole matrix. Furthermore, applying the teaching of Masahiko of scanning the gate lines alternately upwards and downwards (rows or selection lines) to a matrix such as disclosed in Lee, does not solve the problem of gradation along a selection line as is possible with Applicants' claimed invention. Thus, Applicants' claimed invention provides for simpler circuitry and improved performance as compared to Lee, and Masahiko's teaching applied to Lee does not enable Lee to reach such a performance.

Applicants have also considered Kwon and Koyama and submit that neither of these references cure the deficiencies of Lee and Masahiko. Kwon teaches changing a scanning direction of a single line based on a scanning signal DWN.[14] Koyama teaches a synchronous clock signal to change a scanning direction of a single line.[15] Neither Kwon nor Koyama

[12] Masahiko, page 8.
[13] Masahiko, page 9, first paragraph.
[14] Kwon, column 10, lines 64-67.
[15] Koyama, column 8, lines 27-44.

teach or suggest alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines, as recited in Applicants' Claim 1.

Thus, as none of the cited prior art, individually or in combination, disclose or suggest all the elements of independent Claim 1, Applicants submit the inventions defined by Claim 1, and all claims depending therefrom, are not rendered obvious by the asserted prior art for at least the reasons stated above.[16]

Accordingly, in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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[16] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."